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Low-Cost Approach for Integrated Long-Wavelength Infrared Sensor Arrays

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Abstract

A new low-cost process for mid resolution FIR-Arrays for thermal imaging in the LWIR range (8-14µm) has been developed. Integrated array devices with 1k and 5k pixel array size have been designed and manufactured using this process which is fully compatible with semiconductor production. The devices are suitable to support detection of humans e.g. in security and automotive safety applications.

Keywords: MEMS, Sensor, Far-Infrared-Array, Thermal imaging

1. Motivation

Thermal imaging allows the reliable detection of humans in different applications like pedestrian detection in automotive night-vision or intruder detection in security systems. Presently available un-cooled bolometer technologies rely on expensive post-processing of CMOS ASIC wafers and often apply materials or processes not available in semiconductor production flow. The need for dedicated equipment and the lack of applicability of batch wafer-level packaging prohibit further cost reduction with these technologies and thus limit the emergence of new high volume civil applications.

Within the EU FP7 Project ‘ADOSE’ a new technology for cost efficient, mid-resolution infrared arrays sensitive in the 8-14 µm wavelength range is being developed [1]. Detection of the thermal radiation is achieved by an array of suspended mono-crystalline thermo-diodes generated inherently during the read-out ASIC process. Vacuum packaging is done in a batch wafer-level sealing process.

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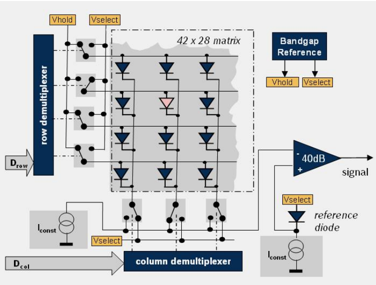


Fig. 1: Simplified schematic of diode matrix and read-out circuit with pixel selected

2. Low-cost thermo-sensor array approach

2.1. Sensitive Element Choice

Standard resistor-based bolometer arrays require the use of a decoupling matrix on top of which the bolometer array structures are deposited and formed. In order to switch to less expensive technologies, diodes were chosen as sensitive elements, because a diode matrix is decoupled intrinsically. Fig. 1 shows schematically a diode pixel selected through row and column addressing. The steps that form a diode are part of every semiconductor process so no non-standard materials or process steps (i.e. special equipment) are required. [2]

2.2. Thermal Isolation of Sensitive Structure

To achieve good sensitivity the sensitive structure needs to be suspended with as less thermal conductivity to the substrate as possible. A technology based on the forming and removal of porous silicon out of the substrate wafer was chosen while most bolometer processes use polyimide or similar materials as a sacrificial layer. The advantage of this will be seen in section 2.4. When using a mono-crystalline epitaxial layer as the functional layer for the electronics, this technology is fully CMOS-compatible. The same technology is already in use for automotive products like pressure sensors, where the epitaxial layer forms a membrane over the cavity that is left behind by the removal of the porous silicon. For the thermo-diode array such a cavity is formed below each pixel and the membrane around the sensitive structure is opened later to optimize the thermal isolation in such way that the sensitive area is suspended by L-shaped beams. To reduce the thermal conductivity of the beams the epitaxial layer is removed in the suspension beam area.

2.3. Absorber

The process chosen contains several layers of silicon dioxide and nitride with an overall thickness of about 4 µm that form an absorbing layer with a mean absorption of above 50%. Dedicated absorber layers like black silicon were examined but not used because they require non-standard process steps and therefore lead away from the low-cost approach of using existing semiconductor technology and equipment.

2.4. Vacuum Encapsulation

A thermo-sensor array needs vacuum encapsulation. Although the pressure sensor using the same process technology is not using a wafer level vacuum encapsulation, the process itself is fully compatible with the standard wafer level packaging technologies that are widely used with other MEMS sensors like acceleration sensors. For the samples a standard glass-frit bonding process with process temperatures in the range of 400-450°C was used. In order to get sufficiently low and stable pressure a SAES standard getter was used inside the wafer cap. With this a cavity pressure of less than 10 Pa could be achieved.

3. Read-out concept

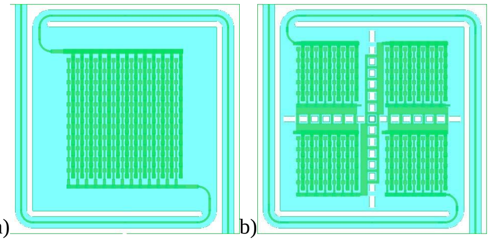
The easiest way to evaluate the junction temperature of a diode is to drive it with a constant current and measure the voltage. In silicon a signal of about -2.2 mV/K can be achieved, depending on the current. With the expected temperature variations of the pixel signals in the order of µ-volts or less and the off-set of the diode of about 500 mV, it is useful to drive a reference diode that is not affected by thermal radiation with an identical current and amplify the difference of the voltages. Fig. 1 shows a simplified schematic of the circuit.

4. Sample Chips and Demonstrator

For a proof of concept an array with 42 by 28 pixels was designed, each with a pixel cavity of 200 by 200 micron. Together with the row and column lines the pixel pitch was 230 µm. As a reference a single pixel with heavily decreased thermal isolation is used. The sensitive area of each pixel consists of two comb-structures covering most of the pixel area. This was done in order to minimize the diode noise. First results showed only noise coming from the read-out IC, so a redesign was done. The redesigned pixels consist of 4 comb-shaped diode structures in epi-Si-blocks separated by etch gaps and connected with metal leads in series. (Fig. 2 shows sample pixels of original and re-design) The series diodes produced a 4 times better SNR than the single diodes and the intrinsic noise of the junction was still not measurable within the noise floor of current source and amplifier.

The read-out IC was placed besides the array, mainly comprising digital address decoders for row and column, a current source with mirror stage and three differential amplifiers. The pixels are grouped in an alternating columns pattern in three groups each relating to one of the amplifiers. The output of the ROIC consists of three analogue signals representing one pixel at a time each.

Additional circuitry like ADC/DAC and power supply was provided on an FPGA-board, were the FPGA was used to transfer the output signals of the chip into a serial USB-signal that send the images to a PC for displaying them. Fig. 3 shows the demonstrator board with attached optics and a sample image. Although the spatial resolution of 42 by 28 pixels is quite low, the images show the potential of the technology when interpolated by a factor of 3.


a) b)
Fig. 2: (a) First pixel design for proof-of concept and (b) after redesign for higher SNR

5. Automotive Array

The proof of concept demonstrator does not meet the automotive night-vision scenario that is targeted in the ADOSE project. To fulfil this, the spatial resolution and the frame rate must be increased. From the scenario we derived an array size of 100 by 50 pixels. In order to keep the size of the array on the chip the pixel pitch was decreased to 100 µm. As the pixel shrink also involved a great loss in absorber area some countermeasures were developed. Besides some minor optimizations of the process regarding smaller leads and etch gaps the two main measures were reduction of ROIC noise and improvement of thermal isolation. The latter was done by switching from metal to poly-silicon as connector material with a result of 5 times better thermal isolation.

The higher frame rate and the lower noise required a more sophisticated evaluation concept, and the concept should be scalable for easy variation of array size. Out of several candidates the concept of using a switched capacitor integration stage per column and a sample and hold stage to serialize the signal seemed most promising, amongst others because of the possibility to trade thermal resolution for temperature range. Fig. 4 shows the design of the automotive 100 x 50 pixel array in comparison to the proof-of-concept. As can be seen, the space consumed by the ROIC has increased largely while the array size could be contained.

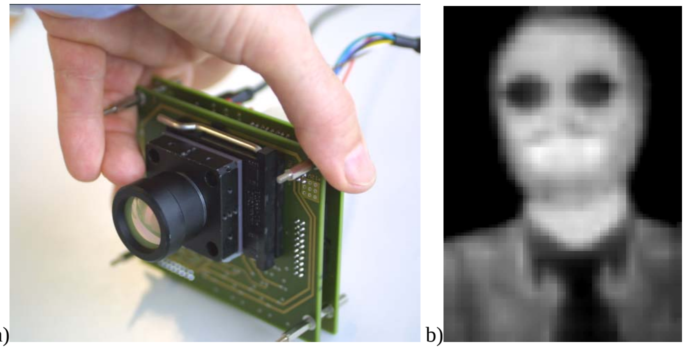

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Fig. 3: a) Photo of the evaluation camera; b) infrared image of a person accessed with the test chip

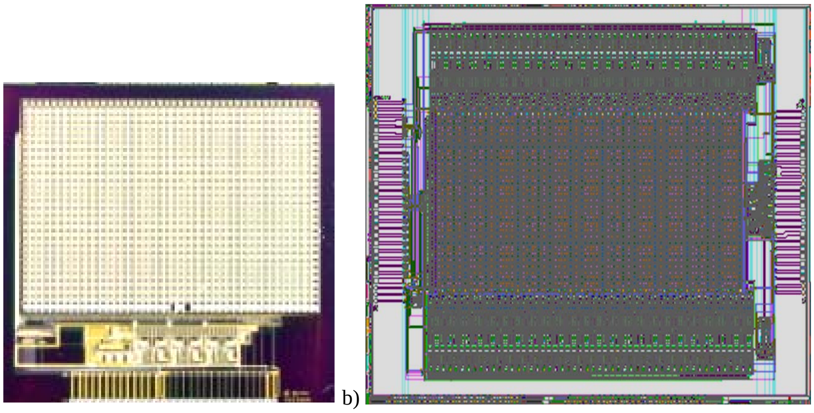
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Fig. 4: a) Proof-of-concept chip; b) design of the integrated 100x50 pixel infrared array under development

Acknowledgements and Outlook

Integrated thermo-sensors with 42x28 array size [Fig. 4a] have been produced to demonstrate the technology and have led to an evaluation FIR-camera [Fig. 3a]. A typical responsivity of >2000 V/W and a NETD of <400mK (@ f/1) have been achieved. A new chip targeting an automotive FIR add-on sensor for use with CMOS NIR vision has been designed next. It implements a faster, low-noise readout ASIC design for the integrated 100x50 pixel array [Fig. 4b]. Development efforts for the sensor design focused on an increase in sensitivity at reduced pixel pitch. Several approaches for further increase in responsivity have been analyzed and should allow finding the best possible performance to cost relation for the packaged sensor fulfilling the specifications. Sample processing is running, implementing a design with four diodes per pixel together with an improved suspension for better thermal insulation and a package with a getter structure in the silicon cap.

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